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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,809	07/30/2003	Hiroshi Shimizu	108397-00107	7790

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EXAMINER	
AUDUONG, GENE NGHIA	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 08/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/629,809	SHIMIZU, HIROSHI	
	Examiner	Art Unit	
	Gene N Auduong	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-9 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-9 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 07-30-03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Braceras (U.S. Pat. No. 6,711,076).

Regarding claim 1, Braceras discloses a semiconductor memory comprising: a plurality of memory blocks each having a plurality of static memory cells (figure 4), a first local bit line connected to the static memory cells (BLT, BLC connected to the SRAM cells), and a first amplifier for amplifying voltage of the first local bit line; a first global bit line (true data line DLT and complementary data line DTC) connected to an output of the first amplifier to transfer read data amplified by the first amplifier of each of the memory blocks; and precharging circuits (precharging devices M14, M16) connected to both ends of the first global bit line (DLT, DLC),

respectively, to precharge the first global bit line to a first power supply voltage (figures 3-4; col. 1, lines 56+; col. 6+, lines 45+; precharging devices M14, M16 precharging the DLT and DTC to a supply voltage).

Regarding claim 2, Braceras discloses the semiconductor memory according to claim 1, wherein the first power supply voltage is an external power supply voltage supplied from the exterior of the semiconductor memory (supply voltage Vdd).

Regarding claim 3, Braceras discloses the semiconductor memory according to claim 1, wherein the precharging circuits each have a first transistor whose gate receives a control signal SAMPRES 40 being activated in a precharge operation, whose drain is connected to the first global bit line (DLT, DLC), and whose source is connected to a first power supply line for supplying the first power supply voltage Vdd (figures 3-4, precharging devices M14, M16).

Regarding claims 4-5, Braceras discloses the semiconductor memory according to claim 3, wherein: the first amplifier has a second transistor whose gate receives the voltage of the first local bit line (one of the gate of the cross coupled sense amplifier circuit receive the voltage of the local bit line), whose drain is connected to the first global bit line (drain of one the cross coupled sense amplifier, which is the output node, connected to the global bit line), and whose source is connected to a second power supply line for supplying a second power supply voltage; and the first transistor of each of the precharging circuits and the second transistor of the first amplifier are inverse in polarity (see figures 3 and 4).

Regarding claim 6, Braceras discloses the semiconductor memory according to claim 1, wherein the memory blocks each have a second local bit line connected to the static memory

cells to transfer data complementary to the data transferred to the first local bit line (figures 3 and 4; also figure 1).

Regarding claim 7, Braceras discloses the semiconductor memory according to claim 1, wherein the first global bit line is laid along the direction in which the memory blocks are arranged (figures 3 and 4).

Regarding claim 8, Braceras discloses the semiconductor memory according to claim 1, further comprising a second global bit line for transferring write data to the static memory cells, and wherein the memory blocks each have a second amplifier for amplifying voltage of the second global bit line and outputting the amplified data to the first local bit line (figures 3 and 4, write data lines DLTW and DLCW).

Regarding claim 9, Braceras discloses the semiconductor memory according to claim 1, wherein the first global bit line is laid in parallel with the first local bit line (figures 3 and 4).

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gene N Auduong whose telephone number is (571) 272-1773.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for

unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GA
August 2, 2004

Gene N Auduong
Primary Examiner
Art Unit 2818